REMARKS/ARGUMENTS

In the Office Action mailed January 24, 2011, claims 1-4, 6, 8, 9, and 11-15 were rejected. In response, Applicant hereby requests reconsideration of the application in view of the below-provided remarks.

For reference, claims 13-16 are amended. In particular, claims 13-15 are amended to depend upon claim 12. Claim 16 is amended to depend upon claim 15. These amendments are supported, for example, by the subject matter described in the specification at page 5, lines 14-25 and the original language of claims 1-5.

Objections to the Claims

The Office Action objects to claims 13-16 under 37 C.F.R. 1.75 as being duplicates of claims 2-5. In particular, the Office Action states that each claim duplicates or is close in content with some other claim of the application.

Court decisions have confirmed applicant's right to restate (i.e., by plural claiming) the invention in a reasonable number of ways. MPEP 706.03(k). Indeed, a mere difference in scope between claims has been held to be enough. Id. Applicant appreciates the Examiner's observation and presents amended claims to address the duplicate issue by no longer depending claims 13-16 upon claim 1. In particular, claims 13-15 are amended to depend upon claim 12. Claim 16 is amended to depend upon claim 15. Accordingly, Applicant respectfully requests that the objections to the claims under 37 C.F.R. 1.75 be withdrawn.

Claim Rejections under 35 U.S.C. 103

Claims 1-6, 8, 9, and 11-16 were rejected based on one or more cited references. The cited reference(s) relied on in these rejections include:

Nakamura (European Pat. Pub. No. 0385404, hereinafter Nakamura)

Day et al. (U.S. Pat. No. 5,887,129, hereinafter Day)

Pohlmeyer et al. (U.S. Pat. No. 6,959,014, hereinafter Pohlmeyer)

In particular, claims 1-4, 6, 8, 9, and 11-15 were rejected under 35 U.S.C. 103(a) as being anticipated by Nakamura in view of Day. Claims 5 and 6 were rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura in view of Day and further in view of Pohlmeyer. However, Applicant respectfully submits that these claims are patentable over Nakamura, Day, Pohlmeyer for the reasons provided below.

Independent Claim 1

Claim 1 is patentable over the combination of Nakamura and Day because the combination of Nakamura and Day does not teach all of the limitations of the claim. Claim 1 recites:

> An electronic circuit arrangement comprising:
> a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal; and
> an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, wherein the asynchronous processor remains dormant in the absence of a clock failure event, wherein the asynchronous processor does not receive and is not dependent on any clock signal.
> (Emphasis added.)

In order to establish a *prima facie* rejection of a claim under 35 U.S.C. 103, the Office Action must present a clear articulation of the reason why the claimed invention would have been obvious. MPEP 2142 (citing *KSR International Co. v. Teleflex Inc.*, 550 U.S. 398 (2007)). The analysis must be made explicit. Id. Additionally, rejections based on obviousness cannot be sustained by mere conclusory statements; instead there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness. Id.

Thus, there are at least three criteria that must be satisfied in order to establish a *prima facie* case of obviousness:

1) The rejection must include a conclusion that the claimed invention would have been obvious.

2) The rejection must include articulated reasoning to support the asserted conclusion of obviousness.
3) The articulated reasoning must be based on some rational underpinning.

Each of these criteria is addressed separately below. In light of the analysis presented below, Applicant submits that the Office Action does not establish a *prima facie* rejection of the claim because the articulated reasoning is not based on a rational underpinning.

1. The rejection must include a conclusion that the claimed invention would have been obvious.

The rejection presented in the Office Action appears to include a conclusion that the claimed invention would have been obvious. With reference to specific language in the claim, the Office Action acknowledges that Nakamura does not teach all of the limitations of the claim. Office Action, 1/24/11, page 3. Hence, the Office Action relies on the combination of Nakamura and Day. Specifically, the Office Action asserts that it would have been obvious to use the invention of Day—having an asynchronous processor that does not receive and is not dependent on any clock signal—in the processor taught by Nakamura. Office Action, 1/24/11, page 3.

It appears that the language of the Office Action is presented as a conclusion that the claimed invention would have been obvious in light of the inventions of Nakamura and Day. Without addressing the validity of this statement, Applicant recognizes that this appears to be a conclusion of obviousness within the scope of the criteria set forth in MPEP 2142.

2. The rejection must include articulated reasoning to support the asserted conclusion of obviousness.

The Office Action appears to articulate reasoning for the asserted conclusion of obviousness. Specifically, the Office Action identifies several elements of Nakamura and Day which purportedly correlate to individual limitations of the claim. For reference, the

following table attempts to summarize the correlations asserted in the rejection presented in the Office Action:

An electronic circuit arrangement comprising: a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal	Nakamura, Figure 1; column 2, lines 42-53.
a processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal	Nakamura, Figure 1; column 2, lines 49-53; and column 3, lines 27-35.
wherein the asynchronous processor remains dormant in the absence of a clock failure event	Nakamura, column 1, line 57 through column 2, line 5.
an asynchronous processor, wherein the asynchronous processor does not receive and is not dependent on any clock signal.	Day, Figure 2; column 1, lines 41-55; and column 4, lines 3-6.

Also, the Office Action states that the reason for the proposed combination of Nakamura and Day is:

> …asynchronous processors provide significant power savings when not doing work.
> Office Action, 1/24/11, page 3.

It appears that the language of the Office Action is presented as a conclusion that the claimed invention would have been obvious in light of the inventions of Nakamura and Day. Without addressing the validity of these statements, Applicant recognizes that this reasoning in the Office Action appears to be articulated reasoning presented in support of the conclusion of obviousness within the scope of the criteria set forth in MPEP 2142.

3. The articulated reasoning must be based on some rational underpinning.

While the Office Action appears to assert a conclusion of obviousness and articulated reasoning in support of that conclusion, Applicant respectfully submits that the articulated reasoning is not based on a rational underpinning. Specifically, the

articulated reasoning lacks a rational underpinning because the reasoning presented in the Office Action is technically deficient to support the proposed combination of cited references. Also, the articulated reasoning lacks a rational underpinning because the reasoning presented in the Office Action is legally deficient to support the proposed combination of cited references.

a. The articulated reasoning in the Office Action lacks a rational underpinning because the reasoning is technically deficient.

In regard to the technical aspects of the proposed combination of Nakamura and Day, Applicant submits that the Office Action does not provide any technical analysis to show how the processor of Day might actually be used with the clock failure recovery system of Nakamura. Although the Office Action makes a general assertion that these inventions might be combined, the modifications that would be necessary to adapt the asynchronous processor of Day for use with the clock failure recovery system of Nakamura are not apparent.

Of particular note is the failure of the reasoning in the Office Action to recognize that controlling the diagnosis processor of Nakamura with the asynchronous processor of Day would result in an inability to execute Nakamura step 95 in Figure 4. Nakamura, column 4, lines 30-32 ("Thus, a failure interrupt from a processor in which a clock failure occurs is inhibited for a predetermined period of time. When such a failure frequently occurs, maintenance is performed in step 95 to cope with this failure."). Because the diagnosis processor of Nakamura must receive some sort of time source in order to execute step 95 in Figure 4, a predetermined time thus must be measured even while the clock components 4 and 5 in Figure 1 are not functioning correctly. Specifically, upon failure of clock components 4 and 5, the Nakamura processor must still be able to measure a predetermined time between failures at a given processor. Thus, Nakamura does not discuss a processor that does not receive any clock signal because some sort of time signal is received at the diagnosis processor. Moreover, introducing a Day processor does not overcome the deficiency of the Nakamura processor because the processor resulting from a combination of Nakamura and Day must still have some sort of time source in order to execute step 95. In other words, even if it were physically

possible to combine the asynchronous processor of Day with the processor of Nakamura, the resulting modified system of Nakamura nevertheless needs to provide the functionality of step 95. Therefore, neither Nakamura nor the combination of Nakamura and Day teach an asynchronous processor that does not receive and is not dependent on any clock signal because the asynchronous processors of both Nakamura and the combination of Nakamura and Day would receive a time source signal.

For the reasons presented above, the articulated reasoning presented in support of the proposed combination of Nakamura and Day is technically deficient to teach all of the limitations of the claim because neither Nakamura nor the combination of Nakamura and Day teach an asynchronous processor that does not receive and is not dependent on any clock signal. Therefore, the articulated reasoning in the Office Action lacks a rational underpinning because the asserted reasoning is technically deficient to show how the proposed combination of the asynchronous processor of Day and the diagnosis processor of Nakamura purportedly might be combined in an operational way. Consequently, the Office Action does not establish a *prima facie* case of obviousness because the articulated reasoning in the Office Action is technically deficient. Accordingly, Applicant respectfully asserts the rejection of claim 1 is improper because the Office Action does not establish a *prima facie* case of obviousness.

b. The articulated reasoning in the Office Action lacks a rational underpinning because the reasoning is legally deficient.

Furthermore, the proposed combination of the inventions of Nakamura and Day would change the principle of operation of the device of Nakamura. In asserting a combination of references as a basis for an obviousness rejection, the proposed combination or modification cannot change the principle of operation of the prior art. MPEP 2143.01(VI).

As explained above, the proposed combination of the diagnosis processor of Nakamura with the asynchronous processor of Day would not result in an operationally functional device. Conversely, if the combination were to rely on a diagnosis processor in Nakamura that received no clock signal, then there would be no need for the diagnosis processor because the step of 95 is apparently maintained by a device other than the

diagnosis processor. Therefore, the inventions of both Nakamura and Day rely on different types of processors that, if combined, would change the principle of operation of the device of Nakamura.

For the reasons presented above, the articulated reasoning presented in support of the proposed combination of Nakamura and Day is legally deficient because the proposed combination would change the principle of operation of the device of Nakamura. Consequently, the Office Action does not establish a *prima facie* case of obviousness because the articulated reasoning in the Office Action is legally deficient. Accordingly, Applicant respectfully asserts the rejection of claim 1 is improper because the Office Action does not establish a *prima facie* case of obviousness.

Independent Claim 6

Applicant respectfully asserts independent claim 6 is patentable over the proposed combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. This claim recites subject matter which is similar to the subject matter of claim 1 discussed above. Although the language of this claim differs from the language of claim 1, and the scope of this claim should be interpreted independently of other claims, Applicant respectfully asserts that the remarks provided above in regard to the rejection of claim 1 also apply to the rejection of this claim.

Independent Claim 12

Applicant respectfully submits that the articulated reasoning for claim 12 does not establish a *prima facie* case of obviousness. Claim 12 recites:

> An electronic circuit arrangement comprising:
> a clock fail circuit arranged to receive a clock signal and to generate an error signal upon an absence of the clock signal; and
> an asynchronous processor arranged to receive said error signal and to bring the electronic circuit arrangement into a pre-defined state upon detection of the error signal, wherein the asynchronous processor remains dormant in the absence of a clock failure event, wherein the asynchronous processor does not consume power in the absence of receiving the error signal.
> (Emphasis added.)

Applicant respectfully asserts independent claim 12 is patentable over the proposed combination of cited references at least for similar reasons to those stated above in regard to the rejection of independent claim 1. Specifically, while the Office Action appears to assert a conclusion of obviousness and articulated reasoning in support of that conclusion, Applicant respectfully submits that the articulated reasoning is not based on a rational underpinning. In particular, the articulated reasoning lacks a rational underpinning because the reasoning presented in the Office Action is technically deficient to support the proposed combination of cited references.

As discussed above, the Applicant submits that the Office Action does not provide any technical analysis to show how the processor of Day might actually be used with the clock failure recovery system of Nakamura. Although the Office Action makes a general assertion that these inventions might be combined, the modifications that would be necessary to adapt the asynchronous processor of Day for use with the clock failure recovery system of Nakamura are not apparent.

As described above, the Nakamura diagnosis processor must receive a time source signal in order to execute step 95 of Figure 4. Nakamura, column 4, lines 30-32 ("Thus, a failure interrupt from a processor in which a clock failure occurs is inhibited for a predetermined period of time. When such a failure frequently occurs, maintenance is performed in step 95 to cope with this failure.") The Office Action does not attempt to explain how this clock signal is received while the processor is not consuming power during the instances where there might be no error signal. Thus, the Office Action does not attempt to explain how step 95 can occur despite the fact that the "asynchronous processor does not consume power in the absence of receiving the error signal," as recited in claim 12 and purportedly taught by the combination of Nakamura and Day. In particular, it is not apparent how Nakamura can receive a clock signal in order to measure a predetermined amount of time, as illustrated in Figure 4. Various methods of measuring a predetermined amount of time are plausible. For example, the diagnosis processor of Nakamura may constantly poll a clock source in order to monitor the predetermined amount of time. In another example, the diagnosis processor of Nakamura may operate synchronously with other components, e.g. by coordinating with other

processors during failure recovery via the left and right arrows of 151, 152, and 153. In such an examples, the combination of the diagnosis processor of Nakamura and the asynchronous processor of Day would not teach an "asynchronous processor that does not consume power in the absence of receiving the error signal" as recited in claim 12 because the combination of Nakamura and Day would result in a processor that consumes power at least during some period where no error signal is being received. Thus, the Office Action fails to explain how the Nakamura diagnosis processor would operate asynchronously, as illustrated by these two examples because the examples describe the need for power consumption while no error signal is received.

For the reasons presented above, the articulated reasoning presented in support of the proposed combination of Nakamura and Day is technically deficient to teach all of the limitations of the claim because neither Nakamura nor the combination of Nakamura and Day teach an asynchronous processor that does not consume power in the absence of receiving the error signal, as recited in claim 12. Therefore, the articulated reasoning in the Office Action lacks a rational underpinning because the asserted reasoning is technically deficient to show how the proposed combination of the asynchronous processor of Day and the diagnosis processor of Nakamura purportedly might be combined in an operational way. Consequently, the Office Action does not establish a *prima facie* case of obviousness because the articulated reasoning in the Office Action is technically deficient. Accordingly, Applicant respectfully asserts the rejection of claim 1 is improper because the Office Action does not establish a *prima facie* case of obviousness.

Dependent Claims

Claims 2-5, 8, 9, 11, and 13-16 depend from and incorporate all of the limitations of the corresponding independent claims 1, 6, and 12. Applicant respectfully asserts each of these claims is allowable based on allowable base claims. Additionally, each of these claims may be allowable for further reasons.

CONCLUSION

Applicant respectfully requests reconsideration of the claims in view of the amendments and the remarks made herein. A notice of allowance is earnestly solicited.

At any time during the pendency of this application, please charge any fees required or credit any over payment to Deposit Account **50-4019** pursuant to 37 C.F.R. 1.25. Additionally, please charge any fees to Deposit Account **50-4019** under 37 C.F.R. 1.16, 1.17, 1.19, 1.20 and 1.21.

Respectfully submitted,

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